REMARKS

The above-identified patent application has been amended and re-examination and reconsideration are hereby requested.

The provisional rejection under the judicially created doctrine of obviousness-type double patenting is acknowledged. The Applicant notes that such rejection is provisional.

Claim1 has been amended to remove the word "section: and therefore is in accordance with 35 USC 112, second paragraph.

Claims 1-12 and 19 stand rejected under 35 USC 103 as being unpatentable over Sandorfi.

Applicant wishes to call the Examiner's attention to FIG. 2 of the patent application. As shown therein, As shown in FIG. 2, the microprocessor interface is coupled between the main memory 48 and the microprocessor 46. More particularly, the microprocessor interface 52 includes a data buffering section 56 coupled to the data port of a microprocessor 46 and a main memory interface coupled to the main memory 48 and also coupled to the data buffering section 56. Referring to Sandorfi, FIG. 1 shows a processor 15P and a system memory 15M, however there is no interface, i.e, a main memory interface and a data rebuffering interface, as claimed) ***between them.***

Referring now to claim 1, such claims points out that the microprocessor interface includes:

> A microprocessor interface ***disposed between a main memory and a microprocessor, such interface*** comprising:
>
> a data rebuffering section adapted to couple data from a one of a plurality of data ports to ***a data port of the microprocessor*** selectively in accordance with a control signal; and
>
> a main memory interface adapted for coupling to a main memory for the microprocessor, such main memory interface being coupled to the data rebuffering section for providing control signals to the main memory for enabling data transfer **between** the main memory and the microprocessor **through the data rebuffering section**. (Emphasis ours)

It is respectfully submitted that Sandorfi does not describe such an interface.

Applicant submits that all of the claims are now in condition for allowance, which action is requested. Please apply any other charges or credits to Deposit Account No. 50-0845.

Respectfully submitted,

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Version of Claims Showing Markings with Changes Made

1. A microprocessor ~~interface,~~interface disposed between a main memory and a microprocessor, such interface comprising:

a semiconductor integrated circuit having formed therein:

(i) a data rebuffering section adapted to couple data from a one of a plurality of data ports to a data port of the microprocessor selectively in accordance with a control signal; and

(ii) a main memory interface adapted for coupling to ~~a~~the main memory for the microprocessor, such main memory interface being coupled to the data rebuffering section for providing control signals to the main memory~~section~~ for enabling data transfer between the main memory and the microprocessor through the data rebuffering section.

2. The microprocessor interface recited in claim 1 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

3. The microprocessor interface recited in claim 2 wherein one main memory type is an SDRAM.

4. The microprocessor interface recited in claim 2 wherein one main memory type is a RDRAM.

5. The microprocessor interface recited in claim 1 including a second integrated circuit adapted for controlling the first- mention integrated circuit, such second integrated circuit having thereon a controller adapted for coupling to the main memory interface, such controller being adapted to produce a main memory access control signal, and wherein:

the main memory has a two portions of addressable locations, one portion being addressed by the main memory interface in response to a preselected range of memory location addresses provided by the microprocessor and the other portion being

addressed by the main memory interface in response to the memory access control signal provided by the controller.

6. The microprocessor interface recited in claim 1 wherein the data rebuffering section includes:

a selector responsive to the control signal for coupling data between a selected one of the data ports and the data port of the microprocessor.

7. The microprocessor interface recited in claim 1 wherein the data rebuffering section includes:

a selector responsive to the control signal for coupling the data port of the microprocessor to either: a selected one of the data ports; or, the main memory, selectively in accordance with the control signal.

8. The microprocessor interface recited in claim 6 wherein the data rebuffering section includes a data distribution unit having a plurality of ports each one of the ports being coupled to a corresponding one of:

(i) the selector;
(ii) a random access memory;
(iii) an interrupt request controller;
(iv) the microprocessor data port; and
(v) the main memory interface.

9. The microprocessor interface recited in claim 8 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

10. The microprocessor interface recited in claim 9 wherein one main memory type is an SDRAM.

11. The microprocessor interface recited in claim 9 wherein one main memory type is a RDRAM.

12. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide the proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

13. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with a control signal provided thereto by the microprocessor to address a selected one of the plurality of potential memory capacities, the control signal supplied by the microprocessor indicating to the main memory controller the particular one of the plurality of potential memory capacities of the main memory.

14. The microprocessor interface recited in claim 13 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

15. The microprocessor interface recited in claim 14 wherein one main memory type is an SDRAM.

16. The microprocessor interface recited in claim 14 wherein one main memory type is a RDRAM.

17. The microprocessor interface recited in claim 14 wherein the main memory interface includes an error correction and detection unit coupled between the distributor and the main memory controller.

18. The microprocessor interface recited in claim 17 wherein the microprocessor is a Power PC microprocessor.

19. The microprocessor interface recited in claim 5 including a mask to transform the address to an address in the second section of the memory.